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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,804	07/18/2003	Lorenzo Bedarida	ATMSP-007	3479

28661 7590 06/29/2004

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EXAMINER	
AUDUONG, GENE NGHIA	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,804	BEDARIDA ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on th cover she t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Objections

2. Claim 2 is objected to because of the following informalities: are there any more limitation following the word "temperature"? If not, the claim should be ended with a period ".". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Mehrotra et al. (U.S. Pat. No. 5,163,201).

Regarding claim 1, Mehrotra et al. disclose a configurable mirror sense amplifier system for flash memory (see figures 5, 9) comprising: a power source generating a reference voltage (figure 9A, col. 11, lines 15+); and an array wherein the array comprises a first plurality of transistors (figures 9A, 9B) and a means for selecting (decoding circuit), each of the first plurality of transistors coupled to the means for selecting (figures 9A, 9B), the array biased at the reference voltage and configured to provide a current for comparison with the flash memory (col. 11, lines 15+; Also anticipated by the Applicant Admitted Prior Art figure 1).

Regarding claim 2, Mehrotra et al. disclose the system of claim 1 wherein the reference voltage is internal, stable and independent from variations of a power supply or temperature (col. 8, lines 22+).

Regarding claim 3, Mehrotra et al. disclose the system of claim 2 wherein each of the first plurality of transistors is in parallel (figure 9B).

Regarding claim 4, Mehrotra et al. the system of claim 3 further comprising a mirror transistor coupled to the array (figures 9A, 9B).

Regarding claim 5, Mehrotra et al. disclose the system of claim 4 wherein a minimum voltage needed for the system is the threshold voltage of the mirror transistor plus the voltage across the array (col. 8, lines 51+).

Regarding claim 6, Mehrotra et al. disclose the system of claim 5 wherein the first plurality of transistors is rapidly switched on (col. 9, lines 20+).

Regarding claim 7, Mehrotra et al. disclose the system of claim 5 further comprising a plurality of sense amplifiers associated with the flash memory and a plurality of arrays, one of each of the plurality of sense amplifiers coupled to one of each of the plurality of arrays (figures 9A, 9B).

Regarding claim 8, Mehrotra et al. disclose the system of claim 5 further comprising a plurality of sense amplifiers associated with the flash memory coupled to the array (figures 9A, 9B).

Regarding claim 9, Mehrotra et al. disclose the system of claim 8 where the plurality of groups of transistors are N-channel transistors (figures 9A, 9B).

Regarding claim 10, Mehrotra et al. disclose the system of claim 9 wherein the first plurality of transistors is configured such that at least one of the first plurality of transistors is activated with a signal in order to provide the current for comparison to the flash memory cell current (figures 9A, 9B, each of the transistors is activated by a signal).

Regarding claim 11, Mehrotra et al. disclose the system of claim 10 further comprising a second plurality of transistors, one of each of the second plurality of transistors coupled to one each of the first plurality of transistors, wherein the second plurality of transistors receive the signal and activate the first plurality of transistors (figures 9A, 9B).

Regarding claim 12, Mehrotra et al. disclose the system of claim 11 wherein the reference voltage is modified in order to modify the current for comparison to the flash memory cell current (col. 11, lines 15+).

Claims 13-16 contain the similar limitation as previously discussed in claims 1-12. Therefore, they are analyzed as previously discussed with respect to claims 1-12.

Regarding claims 17, 18 and 19, the apparatus as previously discussed in claims 1-12 and 13-16 would be performed the method as claimed. Therefore, they are analyzed as previously discussed with respect to apparatus claims 1-12 and 13-16.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA
June 17, 2004

Gene N Auduong
Primary Examiner
Art Unit 2818